

### **REMARKS/ARGUMENTS**

Claims 1-27 are pending in this application. Claims 1, 13, 25, 26, and 27 are independent claims.

Applicant kindly requests favorable reconsideration of the application in view of the following discussion.

### **INTERVIEW**

Applicant thanks Examiner for the interview on 7/27/2006 and the opportunity to discuss this application. In the interview, Applicant and the Examiner were able to determine that the cited reference, Iwasaki, USPN 5,623,417, does not teach or suggest all the claim limitations of the present invention.

Also from the interview, before the Examiner issues a notice of allowance the Applicant needs to clarify a few aspects of the claimed invention. The Examiner asked the Applicant to demonstrate that analog characteristics of "signal transfers" are implicitly disclosed in the specification and claims. Digital characteristics of a signal include actual data being transferred. Analog characteristics include electrical connectivity and waveforms.

The presently claimed invention is a method of automatically creating computer simulations/analyses of signal transfers of a circuit of system design. As background to the present invention, the present invention relates to construction and design of circuits and systems (spec. para. 0002). Computer Aided Design (CAD) and electronic design automation (EDA) tools are used in the circuit design process to describe and analyze the physical arrangement of circuit components and their connections(spec. para. 0004). CAD tools, for example, are used to specify a design for printed circuit boards (PCBs) and the like, by identifying the components to use in a design, their placement, and their inter-connectivity (spec. para. 0004). EDA tools encompass both CAD tools and Computer Aided Engineering (CAE) tools which identify and simulate the electrical behavior of the components and their inter-connectivity(spec. para. 0002).

Also as background to the present invention, to ensure that the components of a circuit or system design will inter-communicate correctly, various types of CAD and EDA tools (i.e., computer simulations) are used to ensure signal integrity and the like (spec. para. 0010). This is because the signals that travel between input/output connections (IOs) or pins are distorted by the electromagnetic effects of the interconnect between the IOs and other physical phenomena or environment conditions (spec. para. 0010). Two typical types of signal integrity analysis are timing analysis and waveform analysis (spec. para. 0010).

In the detailed description of the invention, signal transfers are part of "transfer nets" which include information about functionality, descriptions of nodes and descriptions of electrical connectivity (spec. para. 0035-0036). Signal transfers are identified as number 715 in the detailed description. Paragraph 0037 states:

"Each transfer 715 specifies a source 735 and a receiver 740. A source 735 may have a multiplicity of node IDs 720, though in this example only one is shown. Similarly, a receiver 740 may have a multiplicity of node IDs 720. A source has its corresponding pins send data in an actual design. A receiver has its corresponding pins receive data in an actual design. Though not explicit in the transfer 715, but implicit and derivable therefrom, **an extended net also has "other" types of pins or nodes. "Other" is used to refer to pins that are on the extended net that is driven by a driver but they are not receivers; consequently the "other" pins are subject to the driven electrical signals though they do not utilize them in the transfer.** By inspection of FIGS. 6 and 7A-B conjointly, one can see that the transfers conceptually modeled are described in the transfer net transfers 715."

Also, the detailed description of the invention describes the computer simulations and analyses of signal transfers as "signal integrity simulations" (para. 0046). As previously disclosed, two typical types of signal integrity analysis are timing analysis and waveform analysis. Both of these types of analyses relate to analog analysis. Thus, any person of ordinary skill in the art of circuit design would understand "signal transfers" from the claim language—and support in the written description—to include analog characteristics. If they analysis were only for digital characteristics, then the claim language could have used the term "data transfer". Additionally, the term "signal transfer" inherently includes analog characteristics, while the written description explicitly describes how "signal transfer" includes analog characteristics.

The Examiner also asked Applicant to demonstrate how the claimed "signal transfers" are different from "data transfers" from Iwasaki. Iwasaki focuses on data transfer tools. From the Abstract of Iwasaki, "the unification of the database and the interface permits the unification of functional design automation tools... functional design data is input, and the input functional data is assigned to each functional component stored in a functional component library through a functional component assignment process. The functional data records assigned by functional component are written into a function database by means of corresponding write sections provided in a functional data input interface. The functional data records stored in the function database are read out through corresponding read sections provided in a functional data output interface, whereby arbitrary design tool data is generated at a function level by means of a functional data generation process." The "data transfer" of Iwasaki focuses providing tools to unify the process of transferring data between a database and an interface. Iwasaki is an invention for improving data communication when there exist different data interface tools and formats.

In the present invention, and as discussed above, "signal transfers" include an analog component related to electrical and physical connectivity. Therefore "signal transfers" of the present invention differ substantially from "data transfers" of Iwasaki.

The Examiner also asked the Applicant to show that waveform and timing analysis are an inherent aspect the claim limitations such that no amendment to the claims is necessary. As discussed above, the analysis of "signal transfers" in the claim limitations is a signal integrity analysis. Paragraph 0047 of the detailed description reads:

"In act 1030, **signal integrity analysis** tools may be automatically controlled to analyze the results of the simulations, using the information in the various data structures and lists and possibly using designer specified parameters (e.g., to select the type of analysis, **such as timing analysis** on all receivers, **or waveform analysis** on all nodes). For example, a simulation may be constructed with Cnode driving Mnode 1. Simulation results of each pin may be analyzed using rules determined by both the model data (typically found in an IBIS file) and how the pin is used in the transfer net. Typically overshoot rules would be applied to driver, receiver and other nodes since overshoot is a condition that effects the lifetime of an integrated circuit. Edge rate, and other transition rules would apply at receiver pins only. Monotonic rules might apply at receiver pins of clock nets only. As another example, timing analysis tools may

be triggered to analyze the results of simulation to determine that pre-specified timing constraints are satisfied. The relevant constraints may be checked against the receiver pins of the simulation, as these are the only relevant pins for such analysis.

Because claim language is interpreted in light of the specification, using signal transfer descriptions to construct computer simulations/analyses of physical inter-connectivity encompasses timing, waveform, and other associated analyses.

### **GENERAL DISCUSSION OF IWASAKI**

The relationship between the present invention and Iwasaki is analogous to soccer and baseball. Both soccer and baseball play a game using a ball, but each ball is different in construction, and each sport is different in rules. Likewise, both Iwasaki and the present invention address technology relate to circuits, but each has different construction, use and limitations. More specifically, both disclose transferring data between circuit components, but each teaches different limitations and uses.

Iwasaki describes classifications based on equivalent functions. Addition and multiplication are two high level functions that can be implemented with multiple shift registers hooked up in various ways. Iwasaki recognizes that the function of some groups of shift registers as adders, and some groups of shift registers as multipliers. This is a register transfer view of a digital circuit—kind of a molecular level. The present invention in part is concerned with classifying bits that comprise digital data in these registers. For example, a shift register has data in bits, data out bits, control bits, and clock bits. The present invention classifies each of these bits on each register, not as its function to making an adder or multiplier, but by the physics of how the level of any one bit changes from a 0 to a 1.

By classifying these bits as data in, data out, control, clock, the present invention can determine how to do analog simulation to determine how long it will take a signal to travel from one register to another. In simulating an adder or a multiplier, the present invention may assume the data arrives on time. By knowing how the clocks are distributed to all registers ("providing a description of a physical design of a circuit"), the present invention is able to determine if a signal is at the proper analog level to insure that data gets to a register on time. Whether a register is used in an adder or a multiplier is arbitrary.

Another way to recognize the difference between the two inventions by considering the problem that each invention addresses:

**IWASAKI —**

Problem to Solve: Complicated data communication from variations in data interface tools.

In a common data interface technique, a file of data records, described by a hardware description language, is input to create internal data. There are tools that serve as an interface between an HDL description and internal data. With many variations in tools there are several problems: (1) Changes to HDL specifications mean individual tool revisions; (2) Each tool has its own data format—many tools means a non-uniform system; and (3) with a common database, different formats concurrently exist.

**PRESENT INVENTION —**

Problem to Solve: Inefficient circuit design simulation; design simulation that creates false paths.

One method of simulating and analyzing the behavior of a design is to exhaustively simulate and analyze all interconnections. A designer or tool can cause the simulation and analysis of driving signals to and from nodes to simulate how the component pins behave. This exhaustive approach often causes the simulation of "paths" that in fact are never expected to be used in the actual design. These are known as "false paths." Also, a designer may study the logical design of a system in an attempt to determine whether or not a flagged path is a true or false path (sometimes this option is not practical or available). In either case, these approaches are wasteful of designer time and simulation time, and error prone.

Another approach to simulating design is to have a designer familiar with the logical design of the system architecture construct the appropriate simulations and analyze the resulting waveforms. This approach is wasteful of designer time and error prone. It also requires such analysis to be performed by someone familiar with the logical design and, thus, potentially requires inefficient allocation of engineering talent. Moreover, if a design or component is changed (e.g., substituting one model of processor for another) or is re-characterized (e.g., a modified model is used to more accurately describe electrical

behavior of a component already in the design), the simulations need to be reconstructed and analyzed by the designer.

### COMPLETE RESPONSE TO OFFICE ACTION

According to 35 USC 102, to anticipate an invention, the invention needs to be patented or described in a printed publication. The invention **patented** in Iwasaki—that is what is **claimed** by Iwasaki—does not disclose the presently claimed invention. This is apparent by comparing claim limitations of the two inventions. Thus the next step is to determine whether the specification of Iwasaki **describes** the presently **claimed** invention. Iwasaki does not describe the presently claimed invention as the Office Action suggests.

#### Claim 1 Preamble

On page 2, the Office Action states "Iwasaki anticipates a method and system for functional analysis or simulation of a circuit design." The preamble of claim 1 of the present invention claims the invention as "A method of automatically creating computer simulations or analyses of signal transfers of a circuit or system design."

M.P.E.P. § 2131 states: "A claim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." To anticipate an invention, it is logical that a cited reference would contain several terms (if not each and every) that are identical to what is disclosed in the presently cited invention. A search of Iwasaki shows that Iwasaki fails to disclose many important terms in the presently claimed invention.

The terms "computer simulations", "simulations" and "simulation" and "simulate" are **not** found in Iwasaki. In contrast, these terms appear in the present application 70 times! Part of the focus of the present invention is a method to automate computer simulations. It follows that any reference that could be considered as potentially anticipating would go into some detail about automating computer simulations. It is not possible for Iwasaki to anticipate a method for automating simulations if Iwasaki does not disclose any computer simulations.

The preamble of the present invention also uses the term "analyses" as a synonym for "simulations". A text search of Iwasaki also shows that none of the terms "analyses" "analysis" or "analyze" is found in Iwasaki. In contrast, there are approximately 70

instances of these terms in the present application. It is not possible for Iwasaki to anticipate a method of automating analyses if Iwasaki contains no disclosure of these terms.

The present invention discloses in the preamble that what is being analyzed is "signal transfers". Not once does Iwasaki disclose the term "signal transfer". There is a substantial difference between testing "signal transfers" and providing an interface for "data transfers". The present invention relates to testing analog qualities of digital signals as these signals pass through a transfer net. To test such transfer nets, data used in signals can be arbitrary.

Finally, the preamble of the present invention uses the terms "circuit design" and "system design". A text search of Iwasaki show that Iwasaki discloses neither of these terms. By comparing the preamble of the present invention to Iwasaki, one can see that Iwasaki discloses none of the relevant terms of what the present invention claims. As such, there is no possibility for Iwasaki to explicitly describe the presently claimed invention, and a minute chance to inherently disclose the claimed invention.

It seems logical if one has an invention that—for example—claims a new method of injection molding, then to show that another invention anticipates one would cite patents on methods of injection molding. In the present application, the present invention claims a method of automatically creating computer simulations of signal transfers of a circuit design. The cited reference claims a functional data interface method. Thus, Iwasaki should not be cited against the present invention.

#### Claim 1, First Limitation

The Office Action states that Iwasaki teaches "providing a description of a physical design having physical components, signal transfer between them, component identification, and components connectivity in the design environment" at Figs. 2, 3, col. 1, lines 10-15, col. 4, lines 35-46, and cols. 9 and 10. The Office Action paraphrases this limitation and excludes important clauses. For accuracy, this entire limitation reads: "providing a description of a physical design of a circuit or system having physical components and in which at least one of the physical components may transfer a signal to at least one physical component, wherein the physical design description includes an

identification of the physical components and information descriptive of physical inter-connectivity among the physical components."

Figs. 2 and 3 disclose a functional data interface apparatus and a functional component library. Figs. 2 and 3 are silent on physical design, physical components, physical design description and signal transfer between physical system components. Column 1 lines 10-15 simply discloses background to Iwasaki by disclosing that there exists automated design techniques for logical design and data interface methods. Column 1 lines 10-15 is silent on physical design, physical components, physical design description and signal transfer between physical system components. Column 4, lines 35-46 discusses a module from Fig 3 and that module's functional components and connection among other the functional components. Column 4, lines 35-46 is silent on physical design, physical components, physical design description and signal transfer between physical system components. Cols. 9 and 10 describes functional database storage shown in Figs. 8 and 9. Cols. 9 and 10 are silent on physical design, physical components, physical design description and signal transfer between physical system components.

The portions of Iwasaki, cited for the first limitation of claim 1, were randomly spread throughout the patent document. There is no apparent connection between the cited portions to make any cohesive limitation. Part of the novelty of any invention is the way components are grouped together. Thus any reference that anticipates would have similar elements or steps of a limitation grouped in the same place. By citing terms randomly spread throughout the specification the Office Action appears to be trying to meet claim terms by cutting and pasting.

A text search of Iwasaki on the important terms of this limitation further shows how it is impossible for Iwasaki to anticipate the claimed invention. The following are terms found in the first limitation of the present invention, but NOT FOUND in Iwasaki: "physical", "physical design", "physical components", "transfer a signal", "physical design description", "identification of physical components". Iwasaki also does not disclose information descriptive of physical components. Without disclosing these basic terms that are fundamental to the claimed invention, it is impossible for Iwasaki to anticipate the claimed invention.



Claim 1, Second Limitation

The Office Action states Iwasaki teaches "providing a signal transfer description from source to destination" at col. 4, lines 35-46, and col. 12 line 64 to col. 13 line 67. The actual limitation reads: "providing a signal transfer description for at least one signal transfer, the signal transfer description including a set of source nodes and a set of receiver nodes, wherein the set of source nodes provide the signal to be transferred and the receiver nodes receive the signal transferred from the corresponding set of source nodes, and wherein each node is described by information associated with physical components".

Column 4 lines 35-46 discusses a module from Fig 3 and that module's functional components and connection among other the functional components. Column 4 lines 35-46 is silent on "providing a signal transfer description for at least one signal transfer". Column 4 lines 35-46 is silent on the signal transfer description including a set of source nodes and receiver nodes. Column 4 lines 35-46 is also silent on each node described by information associated with physical components.

Column 12 line 64 to column 13 line 67 discusses data transfers between functional components. It is basically an explanation of Figs. 12 and 13 which shows a functional description for the purpose of explaining the functional data generating process of Iwasaki's invention. Thus, column 12 line 64 to column 13 line 67 is silent on "providing a signal transfer description for at least one signal transfer". Therefore Iwasaki does not teach this limitation.

Claim 1 Third Limitation

The Office Action states Iwasaki teaches "providing a signal transfer description as corresponding to at least a portion of the physical connectivity" at column 13, lines 30-67, and at other areas of the specification. The actual limitation reads: "identifying a signal transfer description as corresponding to at least a portion of the physical inter-connectivity information." Column 13 lines 30-67 discusses data transfers between functional components. It is basically an explanation of Figs. 12 and 13 which shows a functional description for the purpose of explaining the functional data generating process of Iwasaki's invention. Column 13 lines 30-67, and, as discussed above, other areas of the specification are silent on "identifying a signal transfer description as corresponding to at

least a portion of the physical inter-connectivity information." Iwasaki neither discloses signal transfer descriptions, nor physical inter-connectivity information.

#### Claim 1 Fourth Limitation

The Office Action states Iwasaki teaches "using the signal or data transfer description to construct computer simulation/analysis of the connected functional components for verification of the functional design in the physical system design system" at column 1 lines 10-15, column 8 lines 49-60, column 11 lines 5-35, and column 12 lines 30-49. Here the Office Action erroneously construed the claim language. The actual limitation reads: "using information in the corresponding signal transfer description to construct computer simulations or analyses of the corresponding physical inter-connectivity."

The section of the Office Action demonstrates that the Office Action does not understand the presently claimed invention. The Office Action substituted different language for the language of the claimed invention. First, the Office Action substitutes "data transfer" as equivalent to "signal transfer". This is an erroneous substitution. The "data transfer" of Iwasaki relates to interfacing data between databases and other functional components.

The Office Action paraphrases this limitation "to construct computer simulation/analysis of the connected functional components for verification of the functional design." Here also the Office Action erroneously replaces claim language of the present invention with terms from Iwasaki. Instead of discussing simulations of physical inter-connectivity, the Office Action writes of simulation of "connected functional components". The presently claimed invention does not simulate functional components for function design. Instead the presently claimed invention simulates physical interconnectivity.

There is another substantial failure of Iwasaki to describe the presently claimed invention. There is no disclosure in Iwasaki about constructing any computer simulations or constructing any computer analyses. Therefore it is impossible for Iwasaki to anticipate the presently claimed invention. As discussed above, the present invention has ample disclosure of simulations and analyses, while Iwasaki has no disclosure. Therefore Iwasaki does not teach this limitation of the presently claimed invention.

### Claims 2-12

Claims 2-12 depend on independent claim 1. If an independent claim is not anticipated by a reference, then any claim depending from the independent claim is not anticipated by the reference. Claims 2-12 each depend from independent claim 1. As shown above, claim 1 is not anticipated by Iwasaki since Iwasaki does not teach each and every element of claim 1. As dependent claims, claims 2-12 incorporate the limitations of claim 1 by reference and are thus not anticipated by Iwasaki. Therefore, claims 2-12 are patentable over Iwasaki.

### Claim 13

Independent claim 13 is substantially similar to independent claim 1. Claim 1 claims a method and claim 13 claims a system, but both are used for automatically creating computer simulations or analyses of signal transfers of a circuit or system design, and recite substantially similar limitations. As shown above, claim 1 is not anticipated by Iwasaki since Iwasaki does not teach each and every element of claim 1. Likewise, claim 13 is not anticipated by Iwasaki for the same reasons. Therefore, claim 13 is patentable over Iwasaki.

### Claim 14-24

Claims 14-24 depend on independent claim 13. If an independent claim is not anticipated by a reference, then any claim depending from the independent claim is not anticipated by the reference. Claims 14-24 each depend from independent claim 13. As shown above, claim 13 is not anticipated by Iwasaki since Iwasaki does not teach each and every element of claim 13. As dependent claims, claims 14-24 incorporate the limitations of claim 13 by reference and are thus not anticipated by Iwasaki. Therefore, claims 14-24 are patentable over Iwasaki.

### Claim 25 & 26

Independent claims 25 and 26 are substantially similar to independent claim 1. Claim 1 claims a method and claims 25 and 26 claim a computer program product, but all are used for creating computer simulations or analyses of signal transfers of a circuit or system design, and recite substantially similar limitations. As shown above, claim 1 is not

anticipated by Iwasaki since Iwasaki does not teach each and every element of claim 1. Likewise, claims 25 and 26 are not anticipated by Iwasaki for the same reasons. Therefore, claim 25 is patentable over Iwasaki.

#### Claim 27

Independent claim 27 claims a method of validating design libraries having information descriptive of physical components. Like the second limitation of claim 1, the first limitation of claim 27 claims "providing a signal transfer description for at least one signal transfer." As discussed above, Iwasaki does not disclose this limitation. The second limitation of claim 27, "identifying a physical component corresponding to a source node in the signal transfer description", is also not taught by Iwasaki. As discussed above, Iwasaki does not teach or relate to physical components, but instead relates to functional components. The remaining limitations of claim 27 go into further detail on verifying and identifying physical components. The Iwasaki disclosure of functional components does not teach these remaining limitations. Thus Iwasaki fails to teach each and every element as set forth in claim 27 of the present invention. Therefore claim 27 is patentable over Iwasaki.

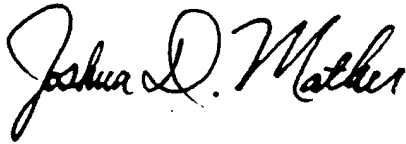
#### **Summary**

Applicant appreciates that the Examiner follows the MPEP by avoiding piecemeal examination by providing all valid grounds of rejection in the first Office Action (MPEP 707.07g). In the first Office Action, the Examiner found no valid §112, or §103 grounds for rejections. The Examiner issued a §102 ground of rejection and asked Applicant to explain how Iwasaki did not anticipate the presently claimed invention. In the above response the Applicant satisfied the Examiner's request by explaining how Iwasaki does not anticipate, and how the claims are fully supported in the specification. Having met the Examiner's request and seeing there are no other valid grounds of rejection, Applicant believes to have demonstrated patentable subject matter, and that the application is in condition for allowance. Applicant kindly requests the Examiner to issue a notice of allowance.

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Reply Dated August 4, 2006  
Reply to Office Action of June 20, 2006  
Atty. Docket No. 04.0152

For all the reasons advanced above, Applicant respectfully submits that the application is in condition for allowance. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully Submitted,

A handwritten signature in black ink, reading "Joshua D. Mather". The signature is written in a cursive style with a large, stylized 'J' and 'M'.

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